REMARKS

Claims 1, 2, 4, 5, and 7-10 are pending in the application. All claims stand rejected.

The Examiner objected to informalities in Claim 10. The informalities have been corrected. The Examiner also rejected Claim 2 under 35 U.S.C. §112, second paragraph, as being indefinite. In reply, Claim 2 was amended as suggested.

The Examiner further rejected Claims 1, 2, 4, 5, and 7-9 under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent No. 5,528,177 ("Sridhar") and Claim 10 as allegedly being anticipated by U.S. Patent No. 5,250,855 ("Asato").

Contrary to the Examiner's statement, however, not each and every element of inventive Claim 1 is present in Sridhar. The third transistor 224 used in Sridhar receives the signal /B, the transistor 446 of the present invention receives the signal B, e.g., "said first transistor receiving a first input signal, said third transistor receiving a second input signal, and said second transistor receiving **an inverse** of said second input signal" recited in Claim 1. Here, the first signal is A, the second signal is B, and the inverse of the second signal is /B.

Claim 1 has been amended to recite: "performing a logic OR operation between a first input signal and inverse of a second input signal, wherein said logic circuit uses silicon-on-insulator (SOI)". In view of this amendment, the Examiner's stated position that input signal /B to Sridhar transistor 224 is equivalent to input signal B to inventive transistor 446 cannot be supported especially in light of the Examiner's position that the circuit outputs are the same. If, as the Examiner insists, the circuits, their inputs and their outputs are the same, then Sridhar transistor 224 and the inventive transistor 446 must use B as input. As the table below shows the difference in the input signal to the third transistor of the Sridhar circuit of FIG. 2g and the inventive circuit of FIG. 2C cannot be ignored. FIG. 2g of Sridhar at node 231 outputs A+B while the inventive circuit shown in FIG. 2C outputs A+/B.

		Sridhar FIG. 2g			FIG. 2C	
			input to		input to	A+/B
A	B	/B	224	231	446	Out
0	0	1	1	0	0	1
0	1	0	0	1	1	0
1	0	1	1	1	0	1
1	1	0	0	1	1	1

It can therefore be concluded that Sridhar does not teach or describe a circuit that can perform an OR operation between signals A and /B or "between a first input signal and inverse of a second input signal" as recited in amended Claim 1.

SOI Discussion

On page 1 line, 15 to page 2, line 5 the present application states that in a Complementary Metal Oxide Semiconductor (CMOS) silicon-on-insulator (SOI) implementation, which is recited in amended Claim 1, threshold voltage drop is minimized and performance is maximized due to the absence of a reverse body effect.

Not only is the SOI implementation of an Negative Channel Metal Oxide Semiconductor (NMOS) transistor body rarely reverse-biased, it tends to be forward-biased with respect to the source. Fluctuating biasing conditions and switching patterns cause a fluctuation in the forward bias of the body-to-source junction of the NMOS transistor, causing large variations in hysteretic delay.

To overcome the drawbacks associated with NMOS only pass-transistor circuits of both bulk CMOS and SOI CMOS implementations, transmission gates using both NMOS and Positive Channel Metal Oxide Semiconductor (PMOS) transistors are used. Very Large-Scale Integration (VLSI) circuits formed of NAND, NOR and INVERTER basic building block circuits using transmission gates are implemented using static or dynamic CMOS.

Static CMOS circuits, used in Sridhar, are generally more widely used due to their superior rail-to-rail voltage swing, robust behavior and high noise immunity. However, static CMOS circuits require one NMOS and one PMOS transistor for every input signal.

Furthermore, static CMOS gates are inverting by nature. This results in a large count of transistors for each basic circuit, large delays, and high power consumption.

The inventive "OR" gate when mapped into SOI, shows improved performance over Sridhar without having the history effect, i.e., there is no parasitic bipolar current. A body potential increasing for both Field-Effect Transistors (FETs) further enhances the performance of the invention. This would not be obvious to these skilled in the art, because this is opposite or counter intuitive to the expected performance.

When transmission gates are mapped into SOI the body potential varies significantly, creating variable delays when input to the gates is switched off. That is why the Positive Channel Field Effect Transistor (PFET), which is "a third transistor for providing an output to be combined with said intermediate signal to create an output signal" recited in Claim 1 of the present invention, would initialize the floating node and avoid the history effect or parasitic bipolar currents.

Floating bodies in SOI for these three transistors help to enhance the performance. Sridhar circuit is slow. The inventive circuit when implemented in SOI, which is a new application to floating body technology (i.e., SOI), is fast with reduced parasitic bipolar currents.

It can therefore be concluded that Sridhar does not teach or describe a circuit for "performing a logic OR operation between a first input signal and inverse of a second input signal" as recited in amended Claim 1. Without conceding patentability per se of dependent Claims 2, 4, 5, and 7-9, these are patentable because of their dependence on Claim 1.

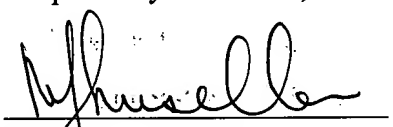
Regarding Claim 10, the transistor 84, and its operation is not described in Asato. In describing its Figure 7, Asato states that the output of NAND gate 72 is applied to a switch 74, which is in a transmitting state if any of signals $A_2, \ldots, A_N$ are in a logic zero state. Asato states only that the embodiment of FIG. 8 differs from the embodiment of FIG. 7 in that the AND gate 71 is replaced by a NOR gate 82, and the NAND gate 72 is replaced by a NOR gate 81.

As discussed with reference to Sridhar, FIG. 8 of Asato receives the inverse of the second

input signal, which in this case is an output of an OR operation of signals $A_2, \ldots, A_N$. Similar to Sridhar, the output of Figure 8 of Asato is A+B while the inventive circuit shown in FIG. 2C outputs A+/B. It can therefore be concluded that Asato does not teach or describe a circuit for an "OR operation performed on said first and the inverse of the second input signals" as recited in amended Claim 10.

In view of the foregoing amendments and remarks, it is respectfully submitted that this application, and all pending claims, are in condition for allowance. Such early and favorable action is earnestly solicited. Should the Examiner have any questions concerning this communication or feel that an interview would be helpful, the Examiner is requested to call the undersigned at the number indicated below.

Respectfully submitted,



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